Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in this application:

Listing of Claims

Claim 1 (currently amended): A system for transmitting data using a network carrying an AC current, comprising:

a timing signal source periodically transmitting phase-coded timing signals comprising one or more phase-coded timing signal symbols and using the AC current to determine when each phase-coded timing signal symbol is transmitted and to phase-code each timing signal symbol;

a plurality of numbered slave units,

each numbered slave unit receiving at least one phase-coded timing signal and using the AC current to determine when each phase-coded timing signal symbol is received and to decode each phase-coded timing signal symbol,

each numbered slave unit transmitting a data signal using its number and time when a timing signal is received to determine when to begin transmitting so that data signals from the slave units do not overlap with each other or with the timing signals; and

a main unit receiving the data signals from the slave units.

Claim 2 (previously presented): The system according to claim 1, wherein, in case of temporary absence of the timing signals, the slave units continue data transmission computing when to begin transmitting using a previously received timing signal.

Claim 3 (previously presented): The system according to claim 1, wherein the timing signal source is not the main unit.

Claim 4 (previously presented): The system according to claim 1, wherein the timing signal is modulated and used to broadcast data from the main unit to the slave units.

Claim 5 (previously presented): The system according to claim 1, wherein all signals being transmitted by the main and slave units have a duration equal to 1/3 of the AC current voltage half-cycle and are centered about zero crossing points of the AC current voltage.

Claim 6 (previously presented): The system according to claim 1, wherein the timing signal source is the main unit.

Claim 7 (previously presented): The system according to claim 1, wherein each timing signal symbol is transmitted over a half-cycle of the AC current voltage.

Claim 8 (previously presented): The system according to claim 1, wherein the start of each timing signal symbol transmission is when the AC current voltage value is zero.

Claim 9 (previously presented): The system according to claim 1, wherein each data signal is transmitted over a half-cycle of the AC current voltage.

Claim 10 (previously presented): The system according to claim 1, wherein the start of each data signal transmission is when the AC current voltage value is zero.

Claim 11 (previously presented): The system according to claim 1, wherein each data signal is transmitted by each N-th numbered slave unit over an N-th half-cycle of the AC current voltage after the end of timing signal.